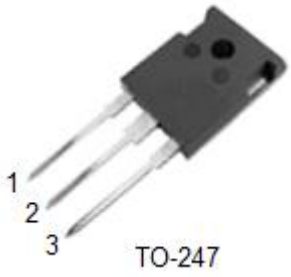
1. Features

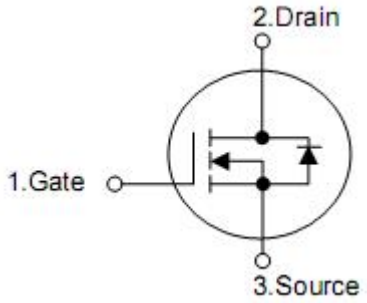
- RoHS Compliant
- $R_{DS(ON),typ.}$=2.4Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- High Voltage Power Supplies
- Capacitor Discharge
- Pulse Circuits

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNM62150A	TO-247	KIA

5. Absolute maximum ratings

(T_C= 25ºC , unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-to-Source Voltage		V_{DSS}	1500	V
Gate-to-Source Voltage		V_{GSS}	±30	
Continuous Drain Current		I_D	11	A
Pulsed Drain Current at V_{GS}=10V		I_{DM}	44	
Single Pulse Avalanche Energy		E_{AS}	350	mJ
Maximum Power Dissipation	T_C=25°C	P_D	312	W
	Derate above 25°C		2.5	W/ºC
Soldering Temperature Distance of 1.6mm from case for 10 seconds		T_L	300	ºC
Storage Temperature Range		T_J&T_{STG}	-55 to 150	

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.4	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	ºC/W

7. Electrical characteristics

(T_J=25°C,unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	1500	-	-	V
Drain-source leakage current	I_{DSS}	V_{DS}=1500V, V_{GS}=0V	-	-	1	uA
		V_{DS}=1200V, T_C=125°C			500	uA
Gate-source forward leakage	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=5.5A	-	2.4	3.2	Ω
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.5	-	4.5	V
Gate Resistance	R_g	f=1 MHz Gate DC Bias=0,Test signal level=20mVopen drain	-	1.19	-	Ω
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz	-	3876	-	pF
Reverse transfer capacitance	C_{rss}		-	170	-	pF
Output capacitance	C_{oss}		-	195	-	pF
Total gate charge(10V)	Q_g	V_{DD}=750V, I_D=11A V_{GS}=0~10V	-	83.2	-	nC
Gate-source charge	Q_{gs}		-	21.6	-	nC
Gate-drain charge	Q_{gd}		-	25.4	-	nC
Turn-on delay time	$t_{d(on)}$	V_{DD}=750V,V_{GS}=10V, R_G=25Ω, I_D=11A		62		ns
Rise time	t_r			188		ns
Turn-off delay time	$t_{d(off)}$			120		ns
Fall time	t_f			158		ns
Continuous Source Current [2)]	I_{SD}	Integral PN-diode in MOSFET			11	A
Pulsed Source Current [2)]	I_{SM}		-	-	44	A
Diode forward voltage	V_{SD}	I_S=11A,V_{GS}=0V,	-	-	1.5	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V,I_F=11A, dI_F/dt=100A/μs	-	449	-	nS
Reverse Recovery Charge	Q_{rr}		-	3.58	-	nC

Note:

1) T_J=+25°C to +150℃

2) Pulse width≤380us; duty cycle≤2%.

8. Test circuits and waveforms

Fig. 1. Output Characteristics @ T_J = 25°C

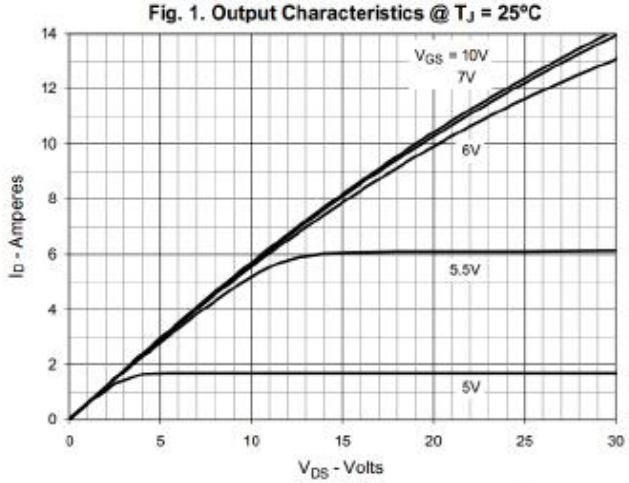


Fig. 2. Output Characteristics @ T_J = 125°C

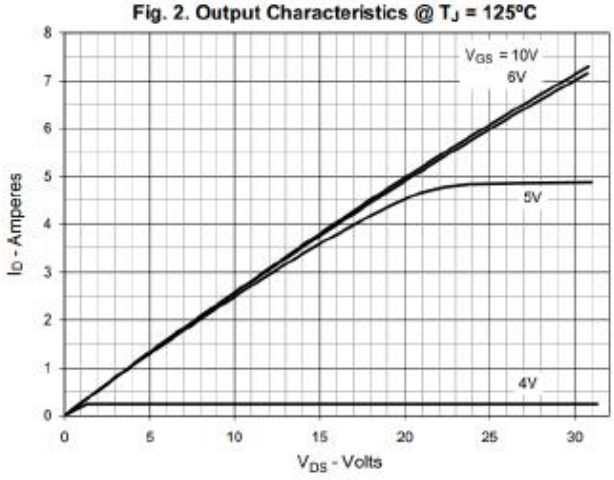


Fig. 3. $R_{DS(on)}$ Normalized vs. Junction Temperature

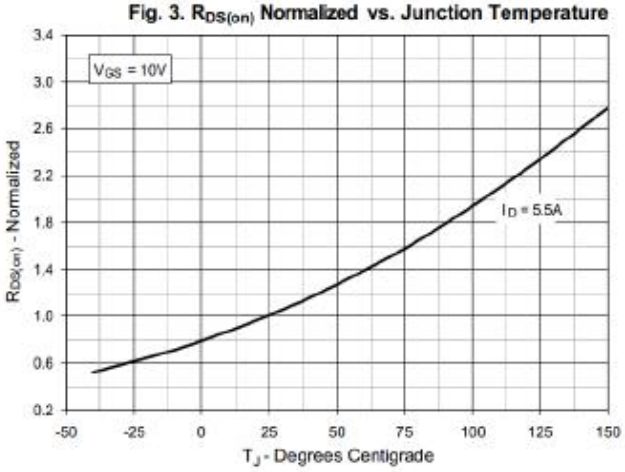


Fig. 4. $R_{DS(on)}$ Normalized vs. Drain Current

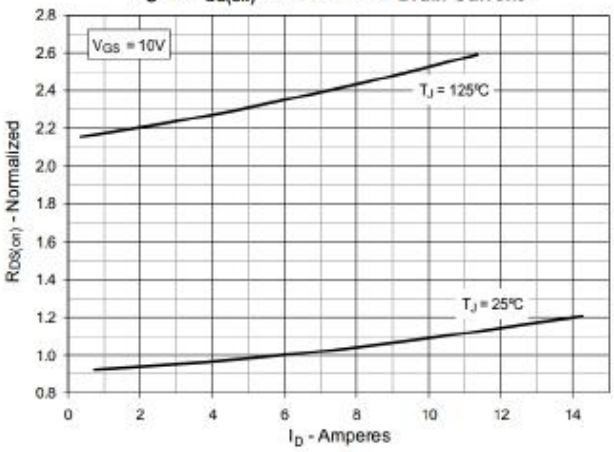


Fig. 5. Maximum Drain Current vs. Case Temperature

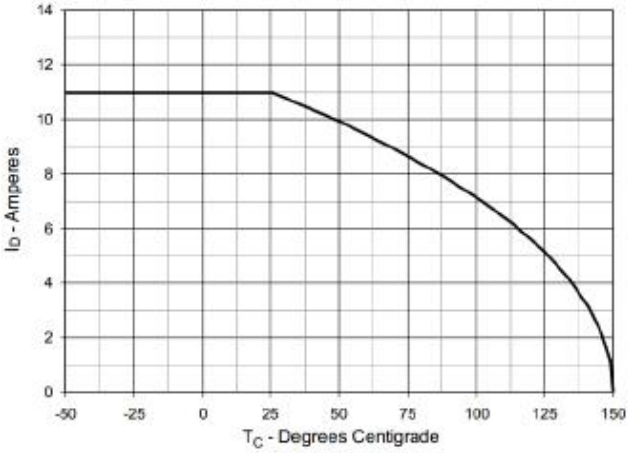


Fig. 6. Input Admittance

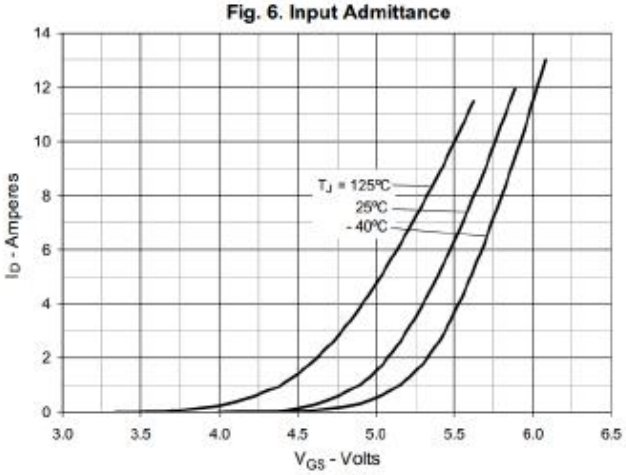


Fig. 7. Capacitance

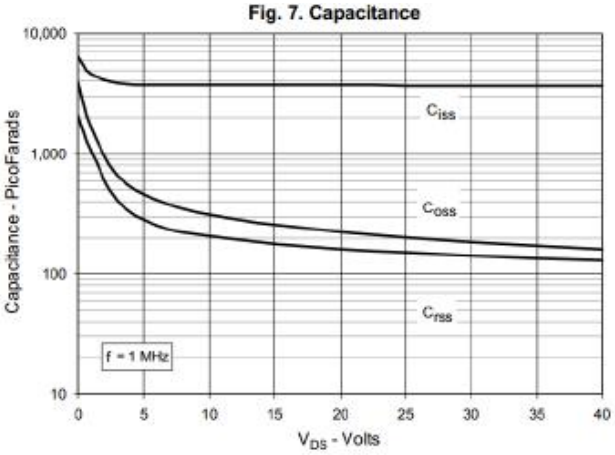


Fig. 8. Forward Voltage Drop of Intrinsic Diode

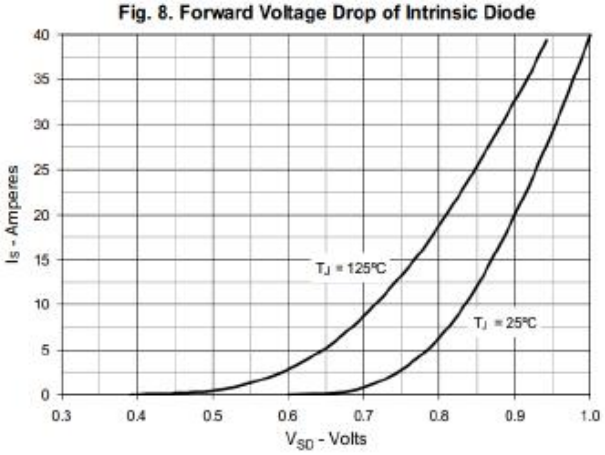


Fig. 9. Gate Charge

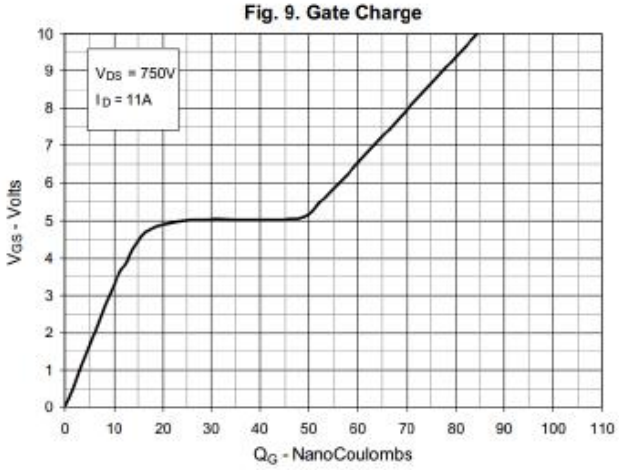
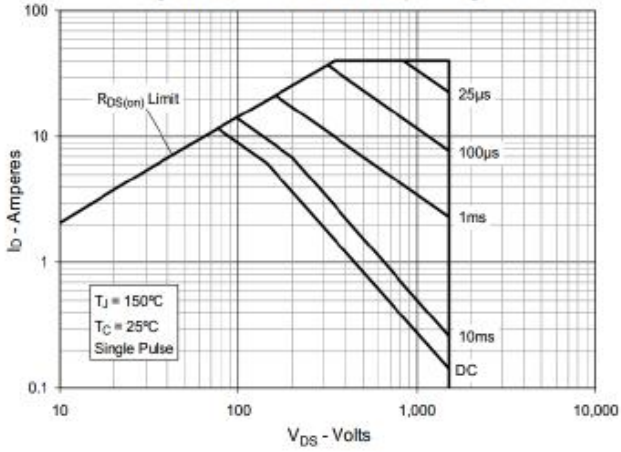


Fig. 10. Forward-Bias Safe Operating Area



9. Test Circuits and Waveform

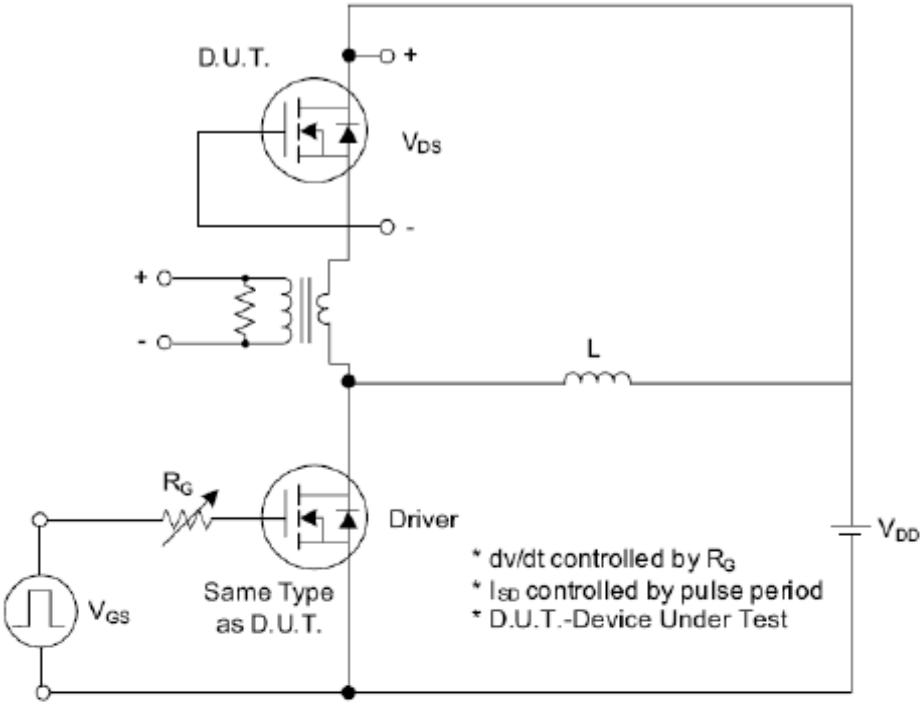


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

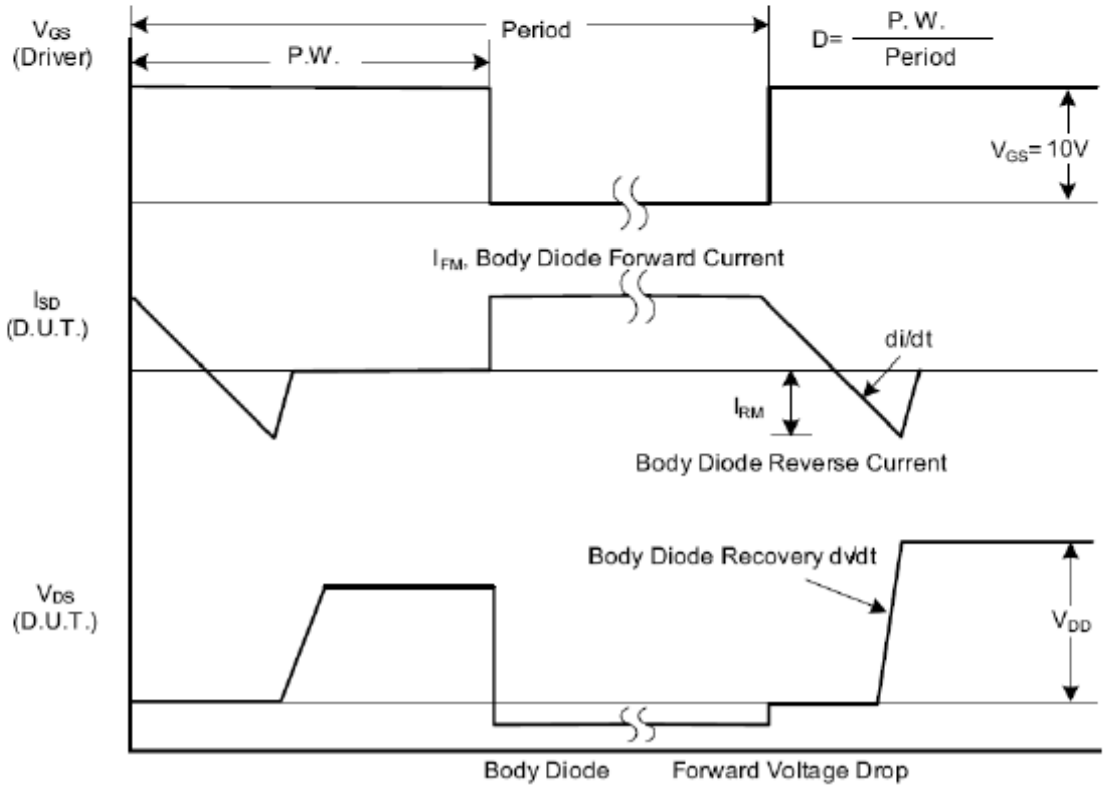


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

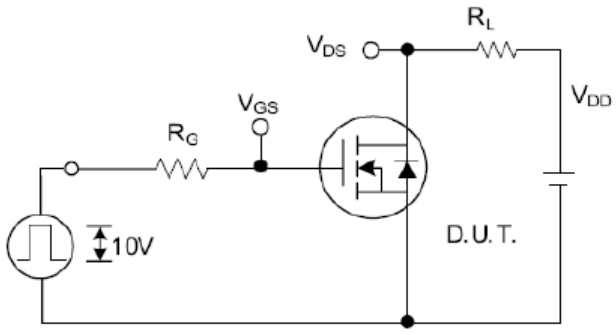


Fig. 2.1 Switching Test Circuit

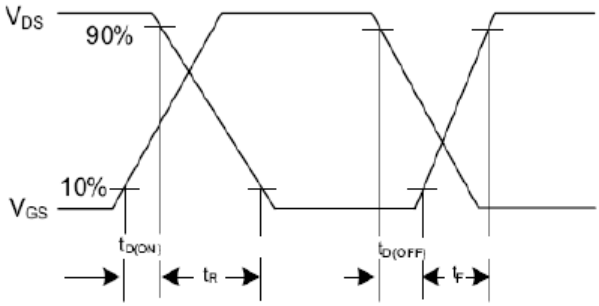


Fig. 2.2 Switching Waveforms

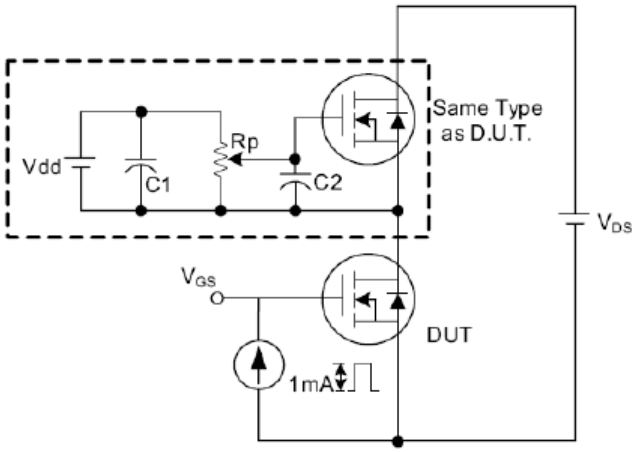


Fig. 3 . 1 Gate Charge Test Circuit

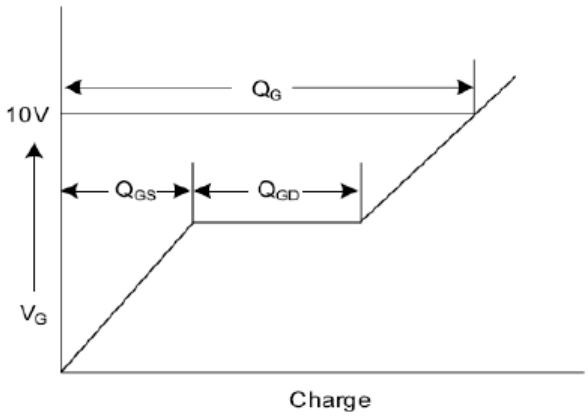


Fig. 3 . 2 Gate Charge Waveform

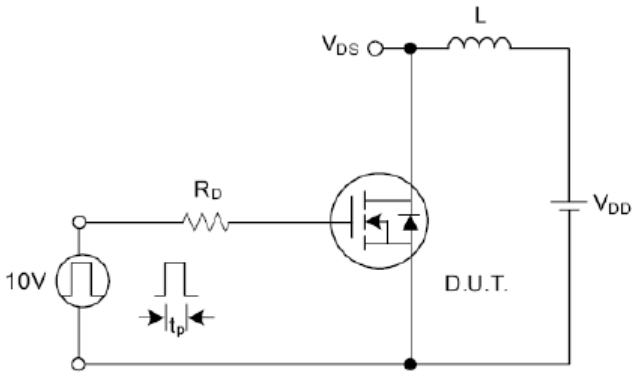


Fig. 4.1 Unclamped Inductive Switching Test Circuit

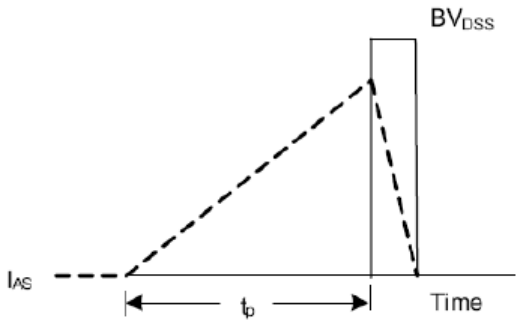


Fig. 4.2 Unclamped Inductive Switching Waveforms