

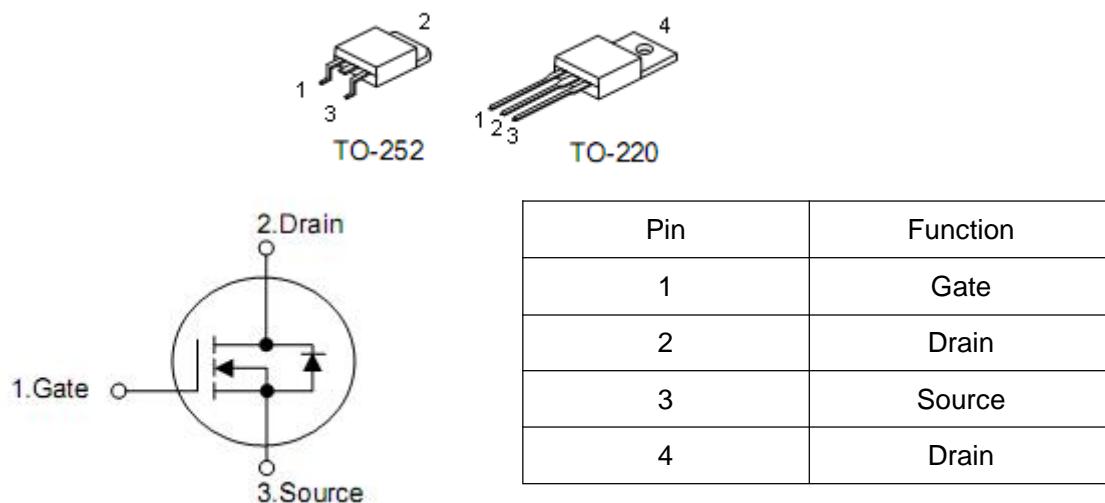
1. Features

- $R_{DS(ON)}$,typ.=9m Ω @ V_{GS} =10V
- 100% EAS guaranteed
- Super low gate charge
- Excellent CdV/dt effect decline
- Advanced high cell density trench technology

2. Description

The KNX3706A is the high cell density trenched N-ch MOSFET ,which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications. The KNX3706A meet the RoHS and Green product requirement, 100% EAS guaranteed with full function reliability approved.

3. Symbol



4. Absolute maximum ratings

Parameter	Symbol	Rating		Units
		TO-252	TO-220	
Drain-source voltage	V_{DS}	60		V
Gate-source voltage	V_{GS}	± 20		V
Continuous drain current V_{GS} @-10V ¹	I_D	50		A
		30		
Pulsed drain current ²	I_{DM}	100		A
Single pulse avalanche energy ³	EAS	72.2		mJ
Avalanche current	I_{AS}	38		A
Total power dissipation ⁴	P_D	52	80	W
Junction and storage temperature range	T_J, T_{STG}	-55 to 150		°C
Thermal resistance-junction to ambient ¹	$R_{\theta JA}$	62	-	°C/W
Thermal resistance-junction to case ¹	$R_{\theta JC}$	2.4	1.56	°C/W

5.Ordering Information

Part Number	Package	Brand
KNP3706A	TO-220	KIA
KND3706A	TO-252	KIA

6.Electrical characteristics

($T_J=25^\circ\text{C}$,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=-250\mu\text{A}$	60	-	-	V
Static drain-source on- resistance ²	$\text{R}_{\text{DS}(\text{on})}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=15\text{A}$	-	9	12	$\text{m}\Omega$
Gate threshold voltage	$\text{V}_{\text{GS}(\text{th})}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	2	-	4	V
Drain-Source Leakage Current	I_{DSS}	$\text{V}_{\text{DS}}=48\text{V}, \text{V}_{\text{GS}}=0\text{V}, T_J=25^\circ\text{C}$	-	-	1	μA
		$\text{V}_{\text{DS}}=48\text{V}, \text{V}_{\text{GS}}=0\text{V}, T_J=25^\circ\text{C}$	-	-	5	μA
Gate-source leakage current	I_{GSS}	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Forward transconductance	g_{FS}	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=30\text{A}$	-	42	-	S
Total gate charge(4.5V)	Q_g	$\text{V}_{\text{DS}}=48\text{V}, \text{V}_{\text{GS}}=10\text{V}$ $\text{I}_D = 15\text{A}$	-	33	-	nC
Gate-source charge	Q_{gs}		-	11	-	
Gate-drain charge	Q_{gd}		-	9.5	-	
Turn-on delay time	$\text{t}_{\text{d}(\text{on})}$	$\text{V}_{\text{DD}}=30\text{V},$ $\text{R}_g=3.3\Omega, \text{V}_{\text{GS}}=10\text{V}$ $\text{I}_D=15\text{A}$	-	10.5	-	ns
Rise time	t_r		-	9.0	-	
Turn-off delay time	$\text{t}_{\text{d}(\text{off})}$		-	65	-	
Fall time	t_f		-	4.5	-	
Input capacitance	C_{iss}	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=15\text{V}$ $\text{F}=1.0\text{MHZ}$	-	2180	-	pF
Output capacitance	C_{oss}		-	255	-	
Reverse transfer capacitance	C_{rss}		-	170	-	
Diode characteristics						
Continuous source current ^{1.5}	I_s	$\text{V}_G=\text{V}_D=0\text{V}$,Force current	-	-	30	A
Diode forward voltage ²	V_{SD}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_s=1\text{A}, T_J=25^\circ\text{C}$	-	-	1.2	V
Reverse recovery time	t_{rr}	$\text{I}_F=15\text{A}, \text{dI}/\text{dt}=100\text{A}/\text{us},$ $T_J=25^\circ\text{C}$	-	19	-	nS
Reverse recovery charge	Q_{rr}		-	15	-	nC

Note:1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width $\leqslant 300\text{us}$,duty cycle $\leqslant 2\%$.
3. The EAS data shows Max.rating. The test condition is $\text{V}_{\text{DD}}=25\text{V}, \text{V}_{\text{GS}}=10\text{V}, \text{L}=0.1\text{mH}, \text{I}_{\text{AS}}=38\text{A}$.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

7. Test circuits and waveforms

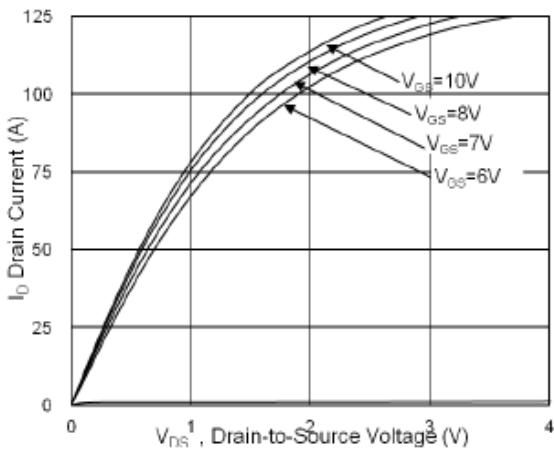


Fig.1 Typical Output Characteristics

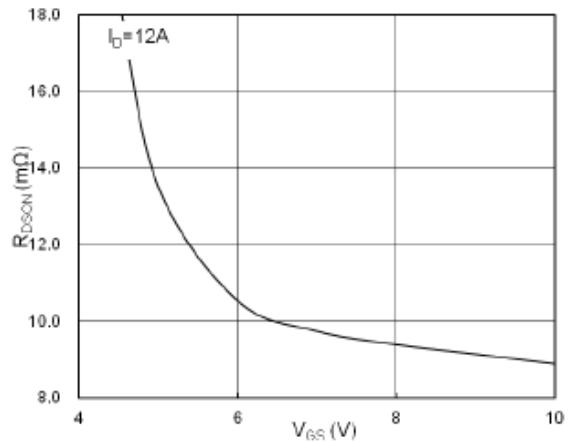


Fig.2 On-Resistance vs. G-S Voltage

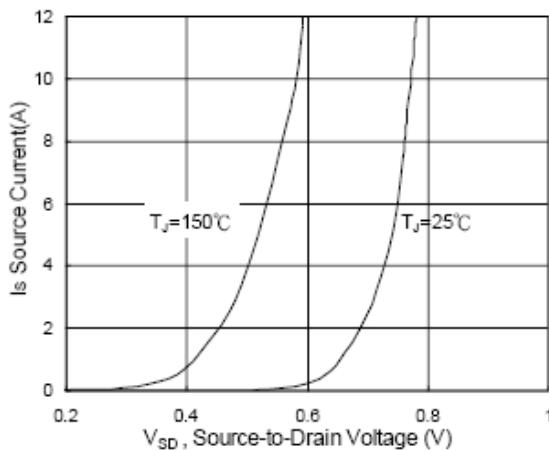


Fig.3 Source Drain Forward Characteristics

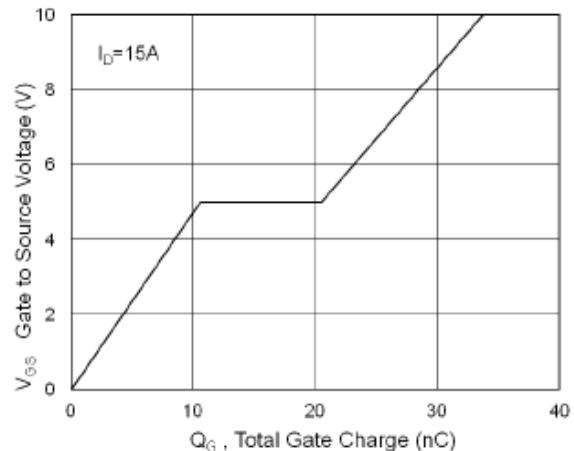


Fig.4 Gate-Charge Characteristics

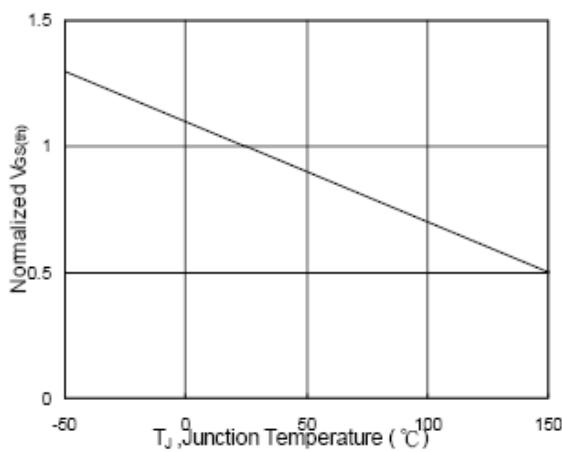


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

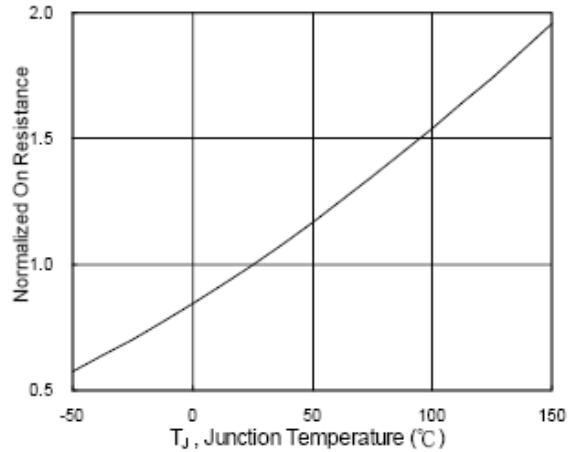


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

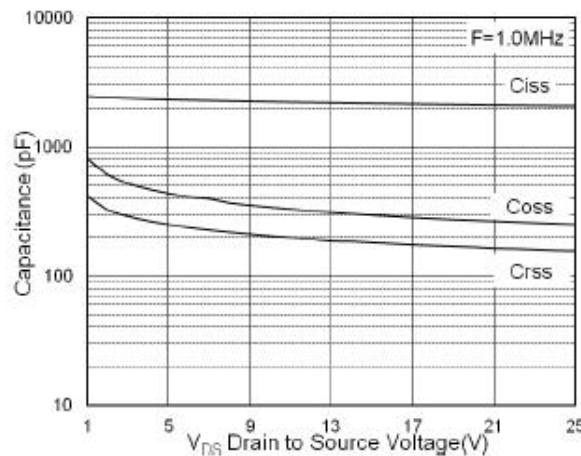


Fig.7 Capacitance

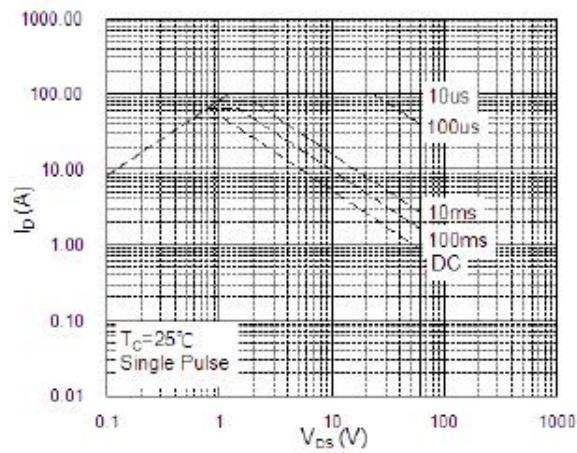


Fig.8 Safe Operating Area

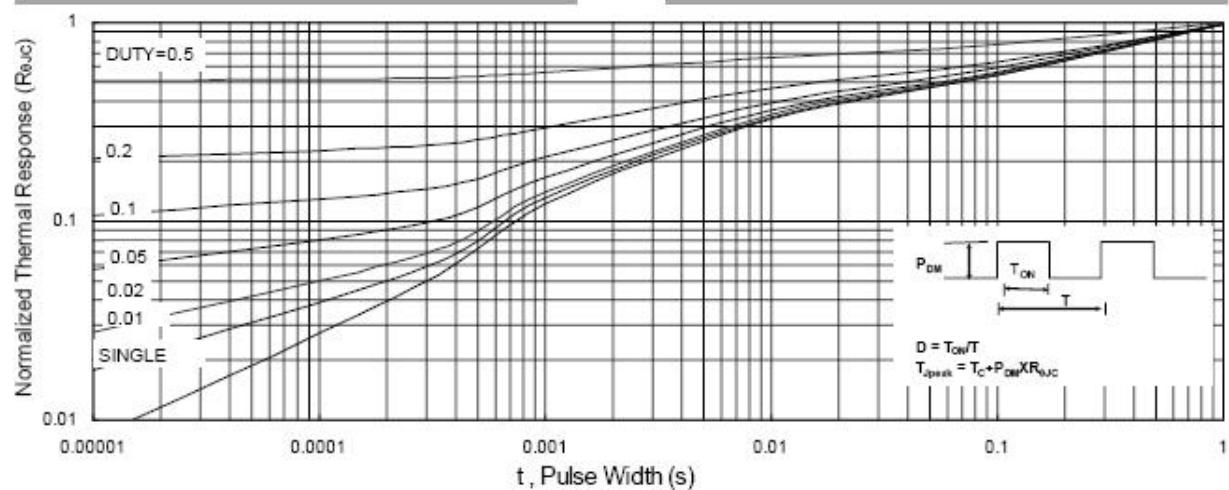


Fig.9 Normalized Maximum Transient Thermal Impedance

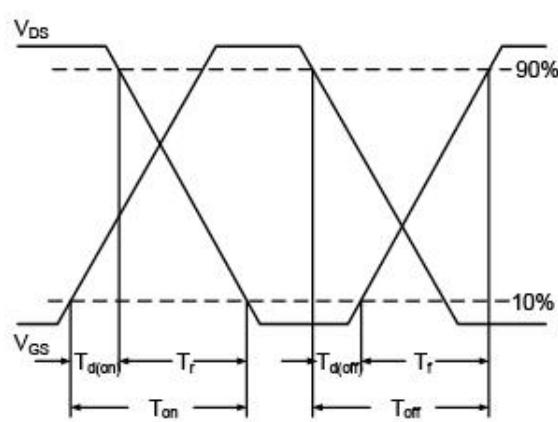


Fig.10 Switching Time Waveform

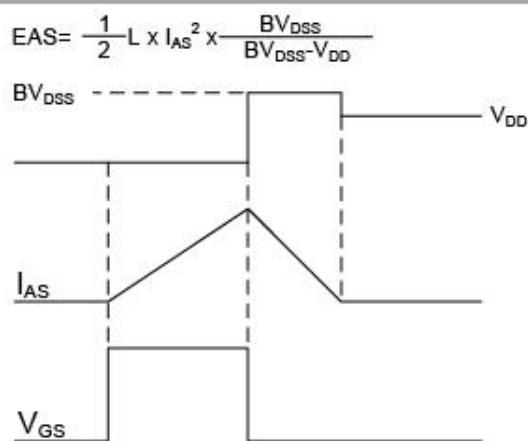


Fig.11 Unclamped Inductive Switching Waveform