

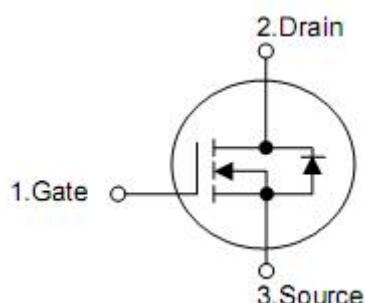
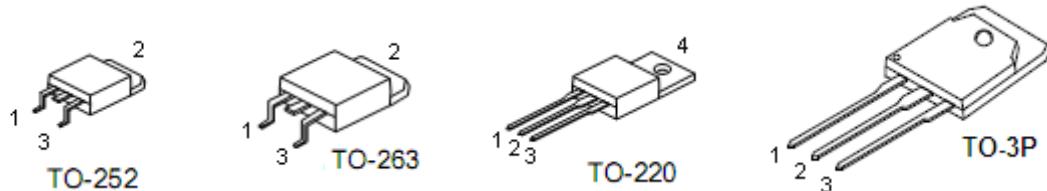
1. Features

- $R_{DS(ON)}=6.5\text{m}\Omega(\text{typ}) @ V_{GS}=10\text{V}$
- Low $R_{DS(ON)}$ to Minimize Conductive Loss
- Low Gate Charge for Fast Switching Application
- Optimized B_{VDSS} Capability

2. Applications

- Power Supply
- DC-DC converters

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KND3206A	TO-252	KIA
KNB3206A	TO-263	KIA
KNP3206A	TO-220	KIA
KNH3206A	TO-3P	KIA

5. Absolute maximum ratings

Parameter	Symbol	Value			Units
		TO-252*	TO-263 TO-220	TO-3P	
Drain-to-source voltage	V _{DSS}	60			V
Continuous drain current	I _D ¹	110*	110	110	A
Pulse drain current @VG=10V	I _{DM}	439*	439	439	A
Power Dissipation	P _D	62	156	185	W
Derating Factor above 25 °C		0.41	1.04	1.23	W/°C
Gate-to-threshold voltage	V _{GS}	±20			V
Single Pulse Avalanche Energy (L=1mH)	E _{AS}	288			mJ
Pulsed Avalanche Energy	I _{AS}	Figure 9			A
Junction & storage temperature range	T _J , T _{STG}	-55~175			°C

*Drain current limited by maximum junction temperature.

6. Thermal characteristics

Parameter	Symbol	Max			Units	Test Conditions
		To-252	To-263 To-220	To-3P		
Junction to case	R _{θjc}	2.42	0.96	0.81	°C/W	Water cooled heatsink, P _D adjusted for a peak junction Temperature of 175 °C

7. Electrical characteristics

($T_A=25^\circ\text{C}$,unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60	-	-	V
Drain-source Leakage Current	I_{DSS}	$V_{\text{DS}}=48\text{V}, V_{\text{GS}}=0\text{V}$ $T_J=125^\circ\text{C}$	-	-	1	μA
			-	-	100	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Gate-to-Source Reverse Leakage						
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=24\text{A}$	-	6.5	8	$\text{m}\Omega$
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2	-	4	V
Diode characteristics						
Diode forward voltage	V_{SD}	$I_{\text{S}}=24\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.4	V
Reverse recovery time	t_{rr}	$I_{\text{S}}=38\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	75		nS
Reverse recovery charge	Q_{rr}		-	100		nC
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=55\text{V}, F=1.0\text{MHz}$	-	3400	-	pF
Output capacitance	C_{oss}		-	430	-	
Reverse transfer capacitance	C_{rss}		-	145	-	
Turn-on delay time	$t_{\text{d(ON)}}$	$V_{\text{DD}}=30\text{V}, I_{\text{D}}=55\text{A}, V_{\text{GS}}=10\text{V}, R_{\text{G}}=2.5\Omega$	-	15	-	nS
Turn-on rise time	t_{r}		-	43	-	
Turn-off delay time	$t_{\text{d(OFF)}}$		-	30	-	
Turn-off fall time	t_{f}		-	10	-	
Gate charge characteristics						
Total gate charge	Q_{g}	$V_{\text{DD}}=30\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=55\text{A},$	-	50	-	nC
Gate-source charge	Q_{gs}		-	20	-	
Gate-drain charge	Q_{gd}		-	15	-	

Note:

1 Calculated continuous current based upon maximum allowable junction temperature $+175^\circ\text{C}$. Package limitation current is 80A.

8. Test circuits and waveforms

Figure 1. Maximum Power Dissipation V.S Case Temperature

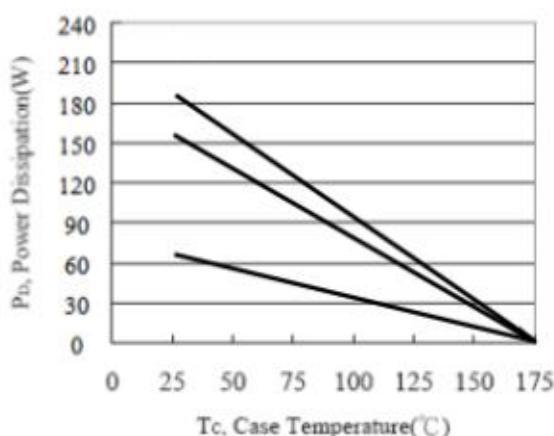


Figure 2. Maximum Continuous Drain Current V.S Case Temperature

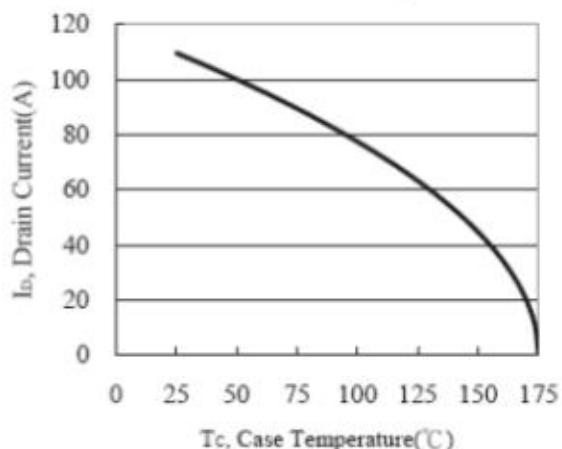


Figure 3. Typical Output Characteristics

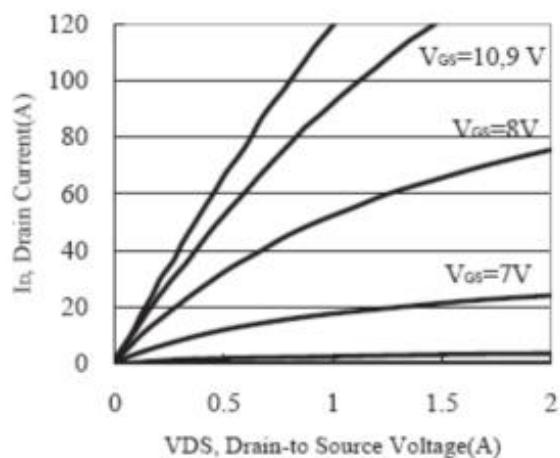


Figure 4. Breakdown Voltage V.S Junction Temperature

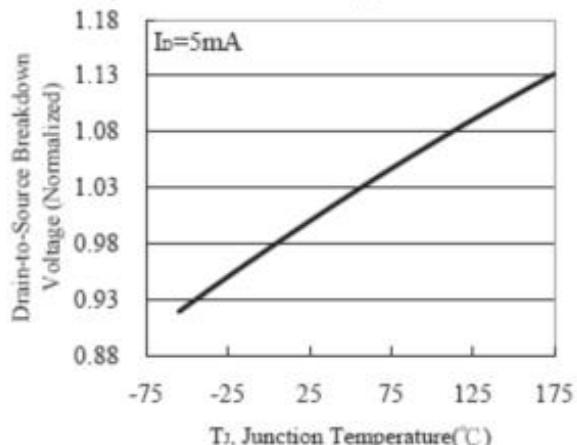


Figure 5. Threshold Voltage V.S Junction Temperature

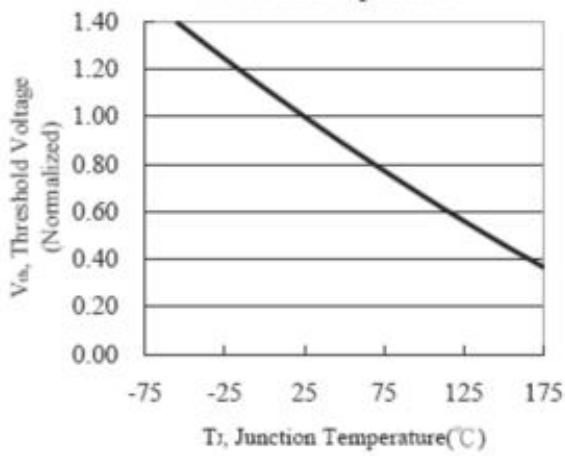


Figure 6. Drain-to-Source Resistance V.S Junction Temperature

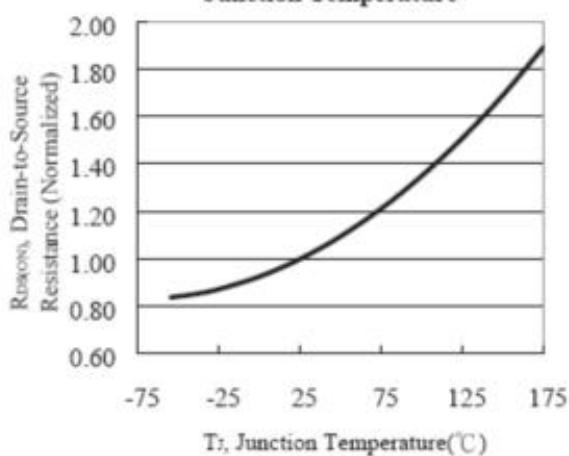


Figure 7. Typical Gate Charge vs. Gate-to-Source Voltage

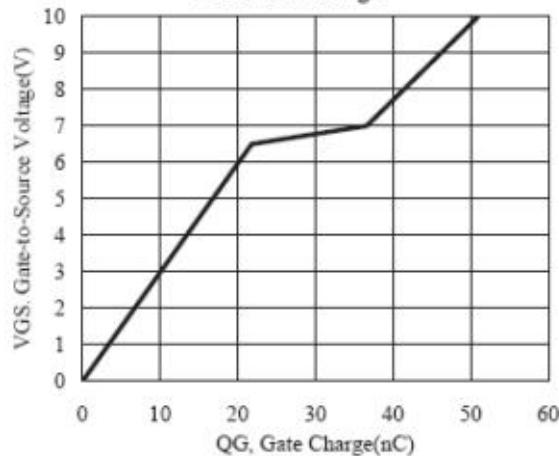


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

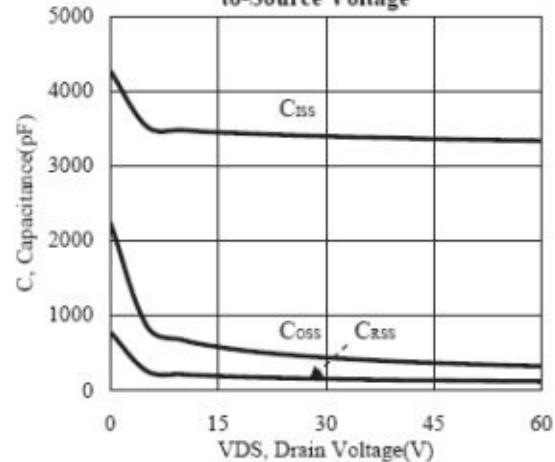


Figure 9. Unclamped Inductive Switching Capability

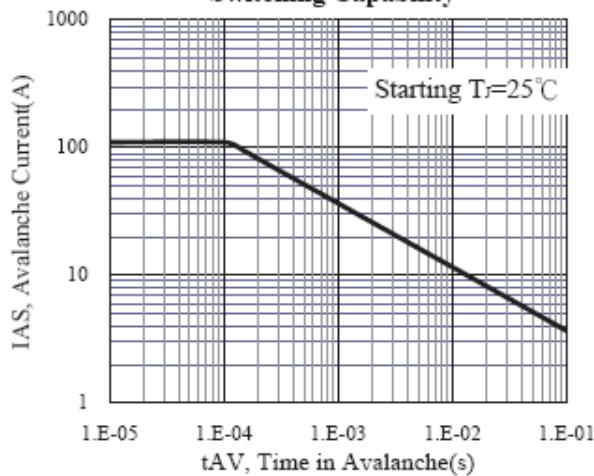
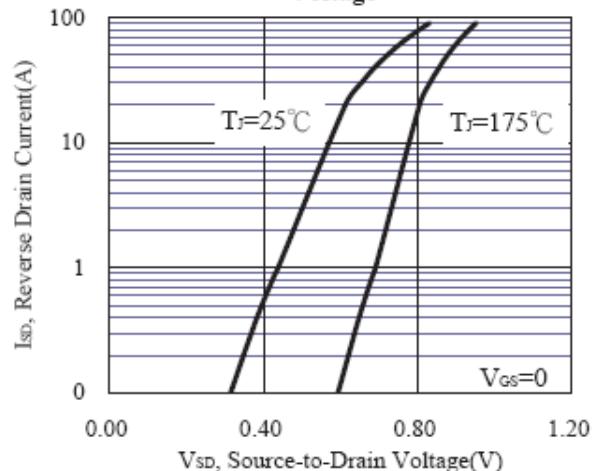


Figure 10. Source-Drain Diode Forward Voltage



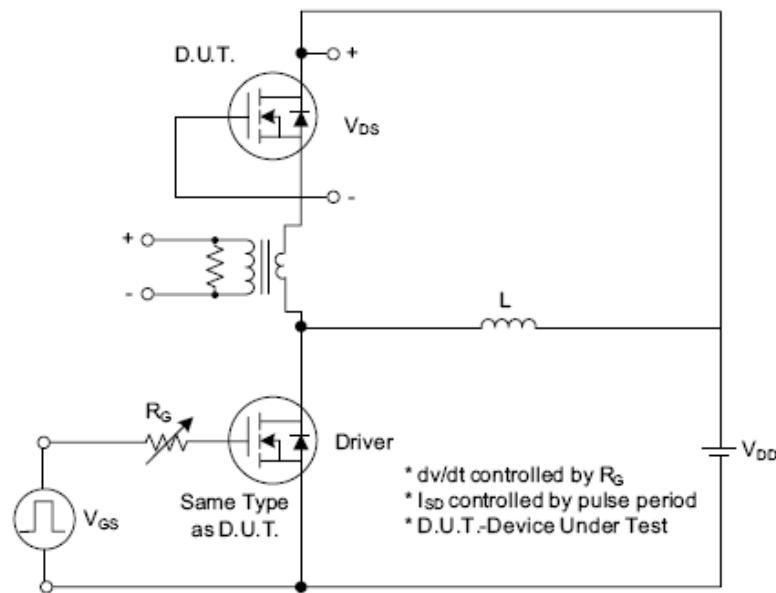


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

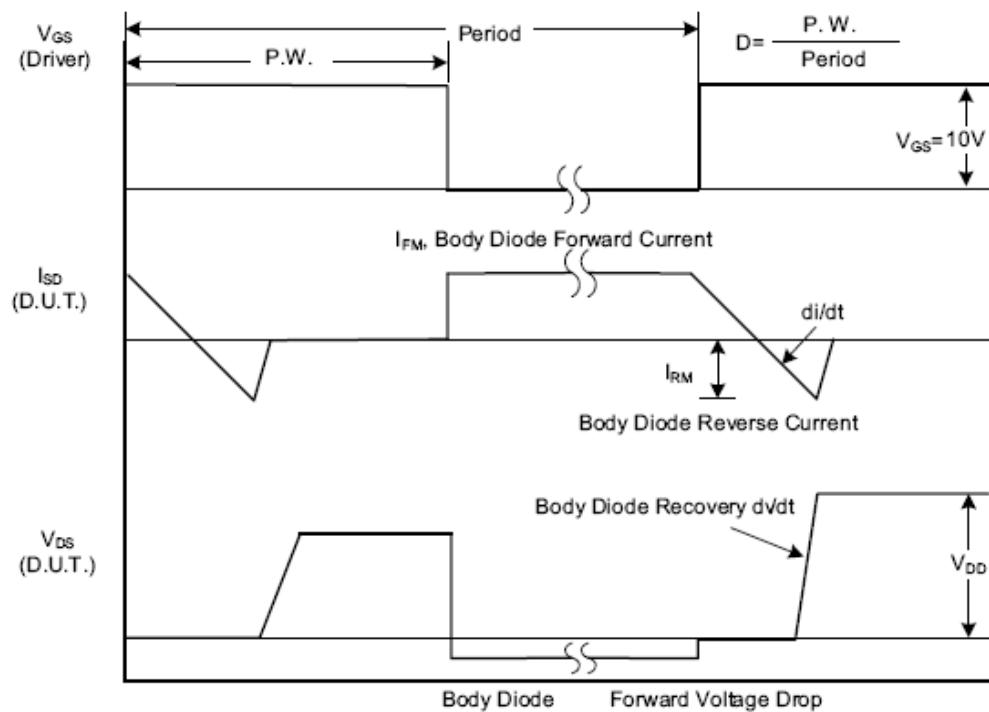


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

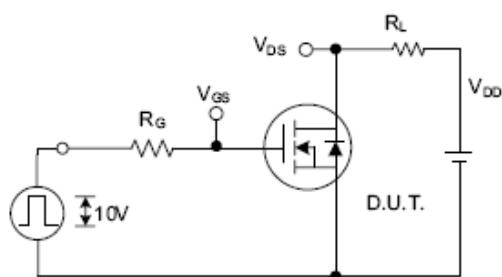


Fig. 2.1 Switching Test Circuit

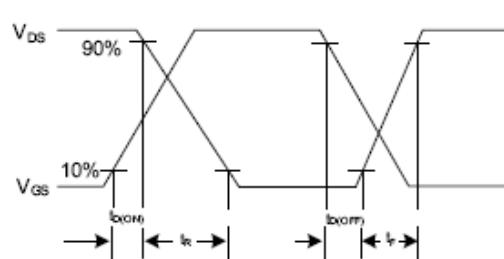


Fig. 2.2 Switching Waveforms

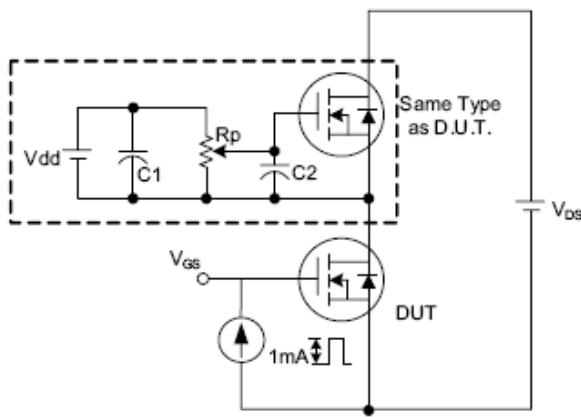


Fig. 3 .1 Gate Charge Test Circuit

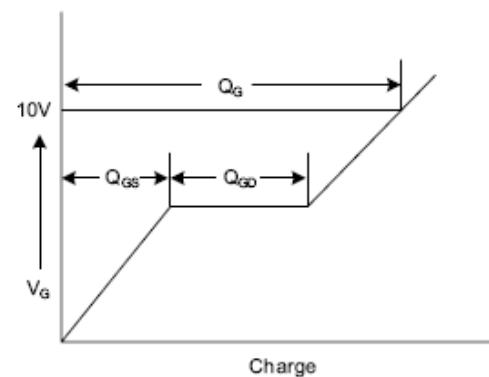


Fig. 3 .2 Gate Charge Waveform

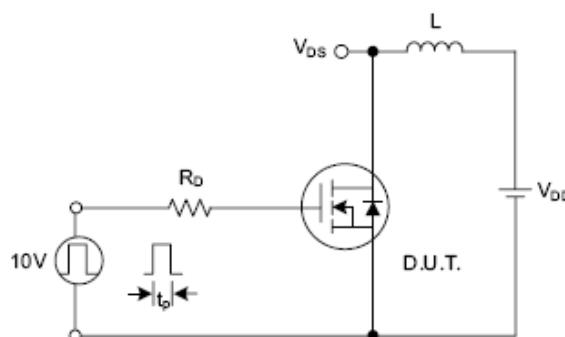


Fig. 4.1 Undamped Inductive Switching Test Circuit

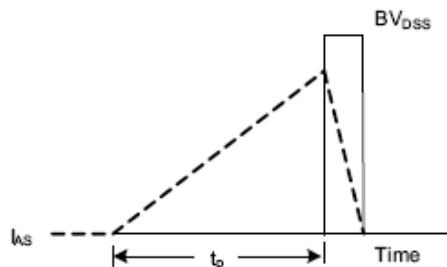


Fig. 4.2 Undamped Inductive Switching Waveforms