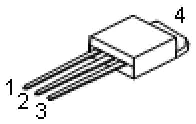
## 1. Description

The KIA8606 is the high cell density trenched N-ch MOSFETS with provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA8606 meet the RoHS and green product requirement, 100% EAS guaranteed with full function reliability approved.

## 2. Features

- Super low gate charge
- 100% EAS guaranteed
- Excellent Cdv/dt effect desline
- Green device available
- Advanced high cell density trench technology

## 3.Symbol



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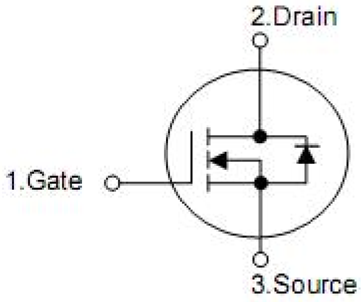


| Pin | Function |
|---|---|
| 1 | Gate |
| 2 | Drain |
| 3 | Source |
| 4 | Drain |

## 4. Absolute maximum ratings

| Parameter | | Symbol | Rating | Units |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 60 | V |
| Gate-source voltage | | $V_{GS}$ | $\pm$20 | V |
| Continuous drain current , $V_{GS}$@10V [1] | $T_C$=25°C | $I_D$ | 35 | A |
| | $T_C$=100°C | | 22 | |
| | $T_A$=25°C | | 7.4 | |
| | $T_A$=70°C | | 6 | |
| Pulsed drain current[2] | | $I_{DM}$ | 80 | |
| Power dissipation[4] | $T_C$=25°C | $P_D$ | 45 | W |
| | $T_A$=25°C | | 2 | |
| Single pulse avalanche engergy [3] | | $E_{AS}$ | 39.2 | mJ |
| Avalanche current | | $I_{AS}$ | 28 | A |
| Operating junction and storage temperature range | | $T_J$ ,$T_{STG}$ | -55 to150 | ºC |

## 5. Thermal characteristics

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Thermal resistance junction-case[1] | $R_{\theta JC}$ | - | 2.8 | ºC/W |
| Thermal resistance junction-ambient[1] | $R_{\theta JA}$ | - | 62 | |

## 6. Electrical characteristics

($T_J$=25°C,unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $BV_{DSS}$ | $V_{GS}$=0V,$I_D$=250μA | 60 | - | - | V |
| $BV_{DSS}$ temperature coefficient | $\triangle BV_{DSS}/\triangle T_J$ | Reference 25℃ $I_D$=1mA | - | 0.057 | - | V/ºC |
| Drain-source on-resistance[2] | $R_{DS(on)}$ | $V_{GS}$=10V,$I_D$=20A | - | - | 20 | mΩ |
| | | $V_{GS}$=4.5V,$I_D$=10A | - | - | 24 | |
| Gate threshold voltage | $V_{GS(TH)}$ | $V_{DS}$= $V_{GS}$,$I_D$=250uA | 1.2 | - | 2.5 | V |
| $V_{GS(TH)}$ temperature coefficient | $\triangle V_{GS(TH)}$ | | - | -5.68 | - | mV/ºC |
| Drain-source leakage current | $I_{DSS}$ | $V_{DS}$=48V, $V_{GS}$=0V $T_J$=25°C | - | - | 1 | μA |
| | | $V_{DS}$=48V, $V_{GS}$=0V $T_J$=55°C | - | - | 5 | |
| Gate-source forward leakage | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| Forward transconductance | gfs | $V_{DS}$=5V, $I_D$=15A | - | 45 | - | S |
| Gate resistance | $R_g$ | $V_{DS}$=0V, $V_{GS}$=0V f=1MHz | - | 1.7 | - | Ω |
| Total gate charge(4.5V) | $Q_g$ | $V_{DS}$=48V, $I_D$=15A $V_{GS}$=4.5V | - | 19.3 | - | nC |
| Gate-source charge | $Q_{gs}$ | | - | 7.1 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 7.6 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=30V, $I_D$=15A, $R_G$=3.3Ω,$V_{GS}$=10V | - | 7.2 | - | ns |
| Rise time | $t_r$ | | - | 50 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 36.4 | - | |
| Fall time | $t_f$ | | - | 7.6 | - | |
| Input capacitance | $C_{iss}$ | $V_{DS}$=15V,$V_{GS}$=0V f=1MHz | - | 2423 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 145 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 97 | - | |
| Continuous source current[1,6] | $I_S$ | $V_D$=$V_G$=0V, Force current | - | - | 35 | A |
| Maximum pulsed current[2,6] | $I_{SM}$ | | - | - | 80 | |
| Diode forward voltage[2] | $V_{SD}$ | $I_S$=1A, $V_{GS}$=0V $T_J$=25°C | - | - | 1 | V |
| Reverse recovery time | $t_{rr}$ | $I_F$=15A,dI/dt=100A/μs $T_J$=25°C | - | 16.3 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 11 | - | nC |

Note:

1. The data tested by surface mounted on a 1 $inch^2$ FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width≤ 300μs, duty cycle ≤ 2%.
3. The EAS data shows max. rating. The test condition is $V_{DD}$=25V,$V_{GS}$=10V,L=0.1Mh, $I_{AS}$=28A
4. The power dissipation is limited by 150 ºC junction temperature.
5. The data is theoretically the same as $I_D$ and $I_{DM}$, in real applications, should be limited by total power dissipation.

## 7. Typical operating characteristics

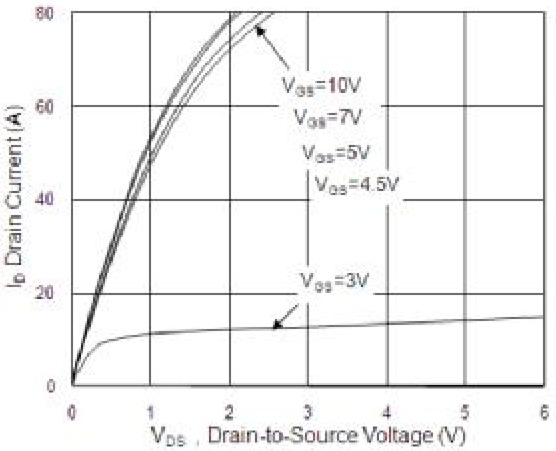


**Fig.1 Typical Output Characteristics**

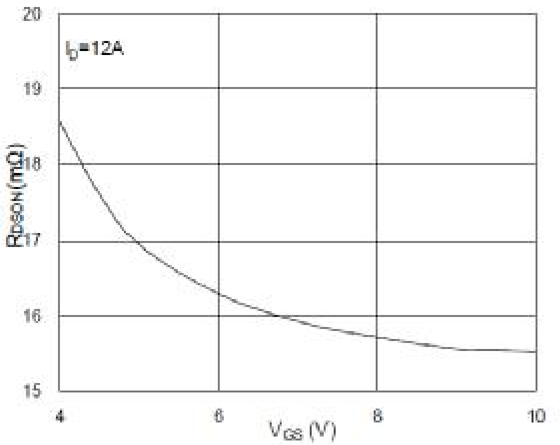


**Fig.2 On-Resistance v.s Gate-Source**

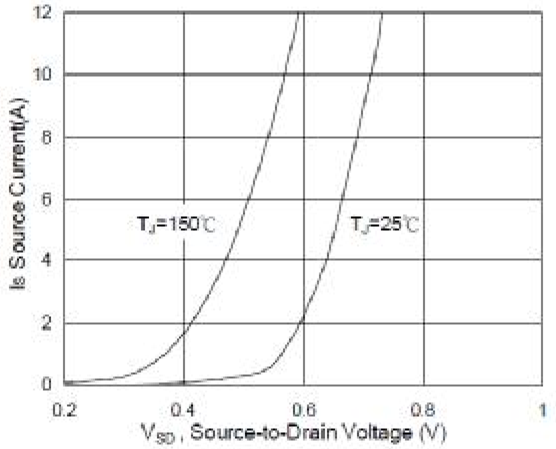


**Fig.3 Forward Characteristics of Reverse**

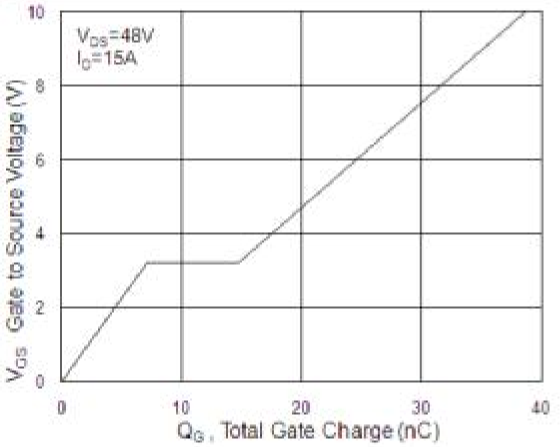


**Fig.4 Gate-Charge Characteristics**

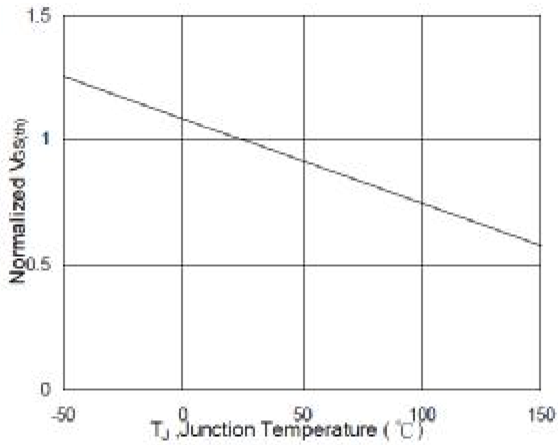


**Fig.5 Normalized $V_{GS(th)}$ v.s $T_J$**

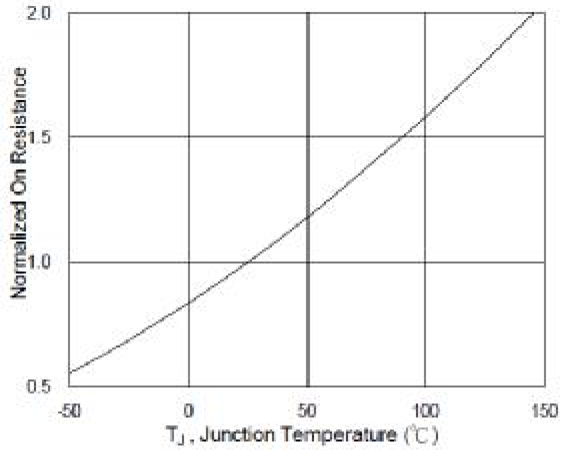


**Fig.6 Normalized $R_{DSON}$ v.s $T_J$**

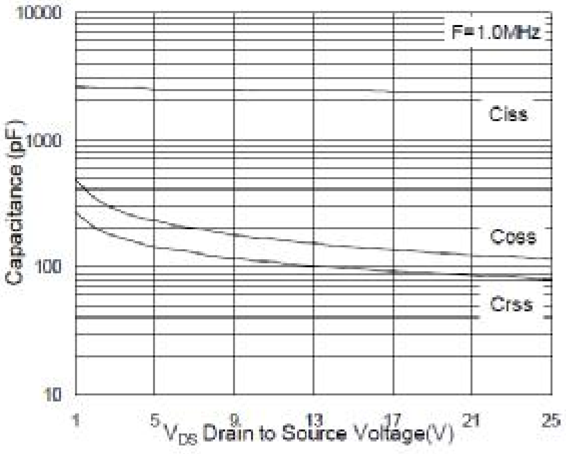


**Fig.7 Capacitance**

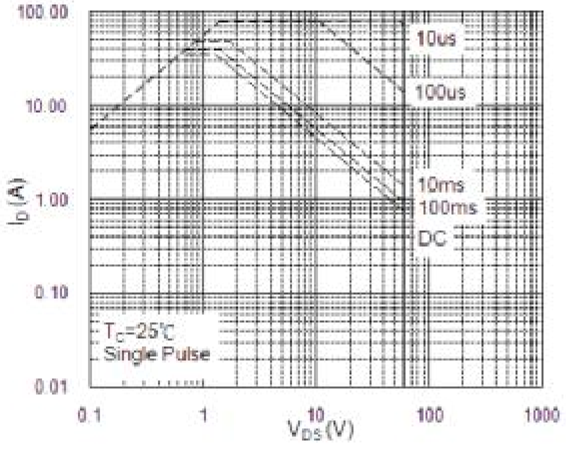


**Fig.8 Safe Operating Area**

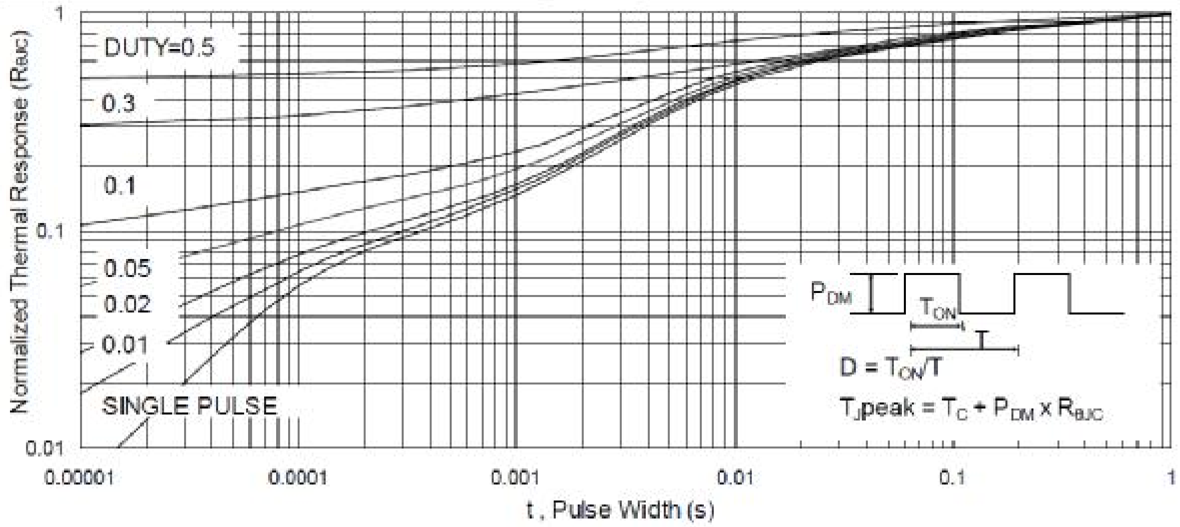


**Fig.9 Normalized Maximum Transient Thermal Impedance**

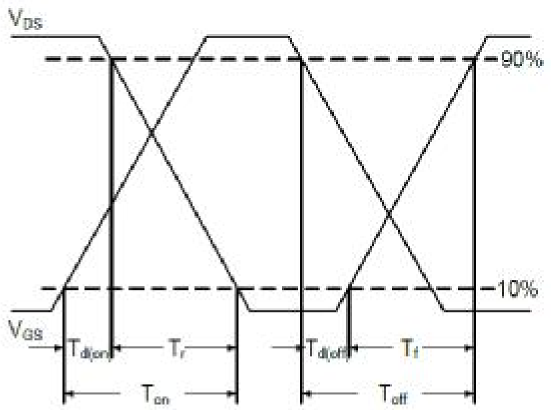


**Fig.10 Switching Time Waveform**

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

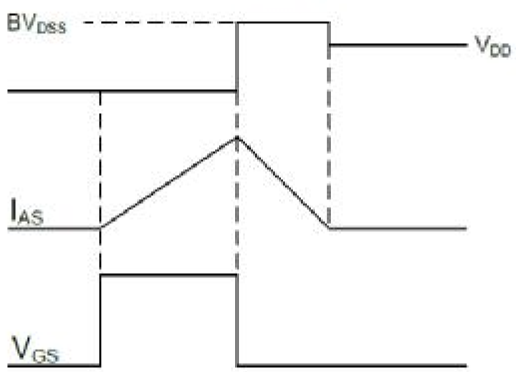


**Fig.11 Unclamped Inductive Switching Waveform**